CLAIMS

What is claimed is:

1. A method for manufacturing a memory, comprising:

forming a first insulating layer on a substrate;

forming a first polysilicon layer over the first insulating layer;

forming a mask layer on the first polysilicon layer;

etching the mask layer to expose portions of the first polysilicon layer, and to define a first patterned region, a second patterned region and a third patterned region, wherein the third patterned region is located between the first patterned region and the second patterned region, the exposed portions of the first polysilicon layer locate in the first patterned region and the second patterned region, and the width of the third patterned region is equal to a predetermined length;

etching the first polysilicon layer to remove the portion of the first polysilicon layer located in the second patterned region;

implanting ions in the substrate to form a first doped region in the second patterned region;

oxidizing the substrate to form a first silicon oxide region in the first patterned region, wherein the first silicon oxide region is formed on the first polysilicon layer;

stripping the mask layer;

etching the first polysilicon layer to form a first gate with using the first silicon oxide region as a mask, wherein the first gate is located in the first patterned

region and is positioned underneath the first silicon oxide region, and a distance between the first gate and the first doped region is equal to the predetermined length; and

implanting ions in the substrate to form a second doped region adjacent to the first gate, wherein the first gate is located between the first doped region and the second doped region.

2. The method of claim 1, wherein the first gate is a floating gate.

3. The method of claim 2, further comprising:

oxidizing the substrate to form a second insulating layer on the first gate;

forming a second polysilicon layer on the second insulating layer; and

etching the second polysilicon layer to form a second gate on the first gate.

4. The method of claim 3, wherein the second gate has a first portion located over the first gate, and a second portion disposed over the second insulating layer and adjacent to the first gate, and the second portion forms a select transistor adjacent to the first gate.

5. The method of claim 1, further comprising:

forming a plurality of spacers on sidewalls of the residual mask layer after the step of etching the mask layer to expose the portion of the first polysilicon layer.

6. The method of claim 1, wherein a photoresist layer and the mask layer are utilized to perform a self-aligned etching process in the step of etching the first polysilicon layer in the second patterned region.

7. The method of claim 6, wherein the photoresist layer and the mask layer are

utilized to perform a self-aligned implanting process in the step of implanting ions in the substrate to form the first doped region in the second patterned region.

8. The method of claim 1, wherein the second doped region is a source, and the first doped region is a drain.

9. The method of claim 1, further comprising:

forming a third polysilicon layer on the first insulating layer; and

forming a third insulating layer on the third polysilicon layer, wherein the first polysilicon layer is formed over the third insulating layer.

10. The method of claim 9, wherein the step of etching the first polysilicon layer in the second patterned region further comprises:

etching the third insulating layer and the third polysilicon layer in the second patterned region.

11. The method of claim 9, wherein the step of etching the first polysilicon layer with using the first silicon oxide region as the mask to form the first gate further comprises:

etching the third insulating layer with using the first silicon oxide region as a mask; and

etching the third polysilicon layer to form a third gate with using the first silicon oxide region as a mask.

12. The method of claim 11, wherein the third gate is a floating gate, and the first gate is a control gate.

13. The method of claim 11, further comprising:

oxidizing the substrate to form a second insulating layer over the substrate;

forming a second polysilicon layer on the second insulating layer; and

etching the second polysilicon layer to form a second gate.

14. The method of claim 13, wherein the second gate is positioned over the first gate and extends at least to a side of the third gate, and the second gate forms a select transistor immediately adjacent to the first gate and the third gate.

15. The method of claim 9, wherein the third insulating layer is an ONO structure insulator.